UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 10/678,893
Filing Date: October 02, 2003
Appellant(s): CHANG ET AL.

MAILED

SEP 2 0 2007

Technology Center 2100

Rodney M. Anderson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/4/2007 appealing from the Office action

mailed 9/19/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings

which will directly affect or be directly affected by or have a bearing on the Board's

decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in

the brief is correct.

(5) Summary of Claimed Subject Mater

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal

Identifies the ground of rejections and the associated claims under rejection to be

reviewed on appeal.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,747,827	Bassett et al.	06-2004
2002/0032891	Yada. et al.	03-2002

| 5,956,743 | Bruce et al. | 09-1999 |
| 6,182,239 | Kramer | 01-2001 |

(9) Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6-7, 9, 11, 16-17, 19, 21, 26, 28 and 31-33 are rejected under 35

U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), and in view of

Yada et al., US Patent Application Publication 2002/0032891).

As to claim 4, Bassett et al. disclose **a method for storing data within a non-**

volatile memory [Error Correction Codes Applied Variably by Disk Zone, Track,

Section, or Content (title); a disk is a type of non-volatile memory] **comprised of a**

plurality of blocks [the storage device is a disk comprising a plurality of zones, tracks

or sectors (title; column 4, lines 17-27)] **in an array formed on a semiconductor**

substrate [the plurality of zones, tracks or sectors are formed in a single disk (title;

column 4, lines 17-27); the aspect of "semiconductor substrate" is taught by Yada, see

below], **each of the plurality of blocks having an indicator indicative of whether**

the block is a reclaimed block [Bessett teaches that the ECC code to be applied to

each of the block depends on an indicator that indicates the attributes associated with

the block (According to a preferred embodiment of the invention, the ECC encoder 40

can encode the data using more than one ECC. The ECC encoder 40 may, for

example, provide two or more ECC coding strategies or algorithms by which the

incoming data may be encoded. The selection of which particular strategy is used may

depend upon a number of factors, below described in detail, depending, for example,

on the radial location on the disk at which the data is to be written, the data type, and

so on (column 3, lines 52-60)); Yada further teaches that each block has an indicator

indicating whether a block is a reclaimed block, see below]; **the method comprising:**

identifying a first block of the plurality of blocks into which data is to be written

[for example, a given zone, track or sector (title; column 4, lines 17-27)];

responsive to the indicator associated with the first block meeting a criterion,

encoding the data using a first error detection algorithm [For example, different

error correcting codes of different strengths may be applied on a sector-by-sector

basis, or on some other basis, depending upon the particular application, data types

involved, and so forth (column 7, lines 29-33); the error correction selection criterion

selects which of said first and second algorithms is to be applied in dependence upon

the physical location of said data on said hard disk drive. In another embodiment, the

error correction selection criterion selects which of said first and second algorithms is

to be applied in dependence upon the type of said data to be written to the disk. The

first and second error correction code algorithms preferably produces a different

number of error correction code bits for application to the data (column 2, lines 37-46);

The method includes applying a first error correction code algorithm to a first set of

data to be written to the hard disk drive. A second error correction code algorithm,

different from the first, is applied to a second set of data to be written to the hard disk

drive. The first and second error correction code algorithms may for example produce

a different number of error correction code bits for application to said data. The

selection between the first and second algorithms may be made, for instance, in

dependence upon the physical location on the hard disk drive to which the data is to be

written, or in dependence upon the type of said data to be written (column 2, lines 15-

26); According to a preferred embodiment of the invention, the ECC encoder 40 can

encode the data using more than one ECC. The ECC encoder 40 may, for example,

provide two or more ECC coding strategies or algorithms by which the incoming data

may be encoded. The selection of which particular strategy is used may depend upon

a number of factors, below described in detail, depending, for example, on the radial

location on the disk at which the data is to be written, the data type, and so on (column

3, lines 52-60); According to a preferred embodiment of the invention, it is observed

that the need for error correction in many applications depends on the frequency and

duration of soft errors, which, in turn, may depend upon the radial position of a given

sector. Thus, two of the salient aspects of the invention are the need for an ECC for

the duration and, frequency of soft errors and the need for an ECC for a given radial

location (column 4, lines 37-45)]; ˙

then writing the encoded data into the first block [When the data is written to the

disk, the ECC bits are typically appended to the end of the sector and become an

integral part of the data in the sector (column 2, lines 3-5)];

identifying a second block of the plurality of blocks into which data is to be written [for example, another given zone, track or sector (title; column 4, lines 17-27)]; **responsive to the indicator associated with the second block not meeting a criterion, encoding the data using a second error detection algorithm** [For example, <u>different error correcting codes of different strengths may be applied on a sector-by-sector basis</u>, or on some other basis, depending upon the particular application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects <u>which of said first and second algorithms</u> is to be applied in dependence upon <u>the physical location</u> of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms preferably produces a different number of error correction code bits for application to the data (column 2, lines 37-46); The method includes applying <u>a first error correction code algorithm</u> to a first set of data to be written to the hard disk drive. <u>A second error correction code algorithm</u>, different from the first, is applied to a second set of data to be written to the hard disk drive. The first and second error correction code algorithms may for example produce a different number of error correction code bits for application to said data. The selection between the first and second algorithms may be made, for instance, in dependence upon the physical location on the hard disk drive to which the data is to be written, or in dependence upon the type of said data to be written (column 2, lines 15-26); According to a preferred embodiment of the invention,

the ECC encoder 40 can encode the data using more than one ECC. The ECC

encoder 40 may, for example, provide two or more ECC coding strategies or

algorithms by which the incoming data may be encoded. The selection of which

particular strategy is used may depend upon a number of factors, below described in

detail, depending, for example, on the radial location on the disk at which the data is to

be written, the data type, and so on (column 3, lines 52-60); According to a preferred

embodiment of the invention, it is observed that the need for error correction in many

applications depends on the frequency and duration of soft errors, which, in turn, may

depend upon the radial position of a given sector. Thus, two of the salient aspects of

the invention are the need for an ECC for the duration and, frequency of soft errors and

the need for an ECC for a given radial location (column 4, lines 37-45)];

the second error detection algorithm having a higher error detection capability

than the first error detection algorithm [for example, the ECC strategies may be

selected to use more ECC bits in association with the data located toward the outer

radii 76 and fewer ECC bits in association with data located toward the inner radii 78

(column 6, lines 21-24)]; **and**

then writing the encoded data into the first block [When the data is written to the

disk, the ECC bits are typically appended to the end of the sector and become an

integral part of the data in the sector (column 2, lines 3-5)];

Regarding claim 4, the invention disclosed by Bassett et al. is applied toward a

disk, which may or may not be formed in a semiconductor substrate. Also, Bassett does

not teach that the indicator is indicative of whether the block is a reclaimed block.

However, the method disclosed by Bassett et al. is equally applicable to a plurality of blocks of memory formed in a semiconductor substrate, because ECC codes are equally applicable to disk-based memory as well as semiconductor-based memory.

Further, Yada et al. disclose in their invention "Data processing System and Data Processing Method" a method of applying different ECC algorithms to different blocks of a flash memory array that is formed on a semiconductor substrate [figure 3(A)~3(D) show the configuration of the flash memory array formed on a semiconductor substrate; The data processing system can be implemented as a single chip type microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip (paragraph 0031); According to the above, the addition of ECC codes and an error correction are performed to increase the number of rewrite assurances with only an access to data stored in <u>a specified partial storage area</u> of a non-volatile memory as an object. Frequently-rewritten parameter data is stored in the specified partial storage area, and program data or the like low in rewriting frequency are stored in other storage areas (paragraph 0029); The present inventors have paid attention to the difference between the individual memory cell characteristics and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use

efficiency of the storage area is set to the maximum (paragraph 0012)].

Moreover, Yada teaches that each block is associated with an indicator indicative

whether a block is a reclaimed block [According to the above, the addition of ECC

codes and an error correction are performed to increase the number of rewrite

assurances with only an access to data stored in a specified partial storage area of a

non-volatile memory as an object. Frequently-rewritten parameter data is stored in the

specified partial storage area, and program data or the like low in rewriting frequency

are stored in other storage areas (paragraph 0029); here the Examiner interprets "a

reclaimed block" as "a reused block." Yada teaches that each block/area is associated

with an indicator indicative of if and how frequently a block/area has been reused

through rewriting].

It is further noted that the inventions of both Bassett et al. and Yada et al. are

directed toward applying different ECC algorithms to different blocks of memory

according to the attributes of each block so that the overhead associated with the ECC

code can be reduced and the memory space can be used more efficiently [Bassett

(abstract; column 1, lines 50-64); Yada (abstract; paragraphs 0029-0030)]. The

invention of Bassett et al. is directed toward disk-based memory while the invention of

Yada et al. is directed to memory based on semiconductor substrate.

Memory based on semiconductor substrate has at least the advantage in terms

of the size when compared to memory based on disk, and can be made of a single

chip [Yada, paragraph 0031].

Providing an indicator indicative of whether a block is a reclaimed block and how

many times the block has been reused is critical in determining the performance and

reliability of a block, as Yada et al teach that the performance of a flash memory is

degraded with an increase in the number of rewriting [paragraphs 0002 and 0005], and

would necessitate the applying of a ECC code to mitigate the degradation [paragraph

0004].

Therefore, it would have been obvious for one of ordinary skills in the art at the

time of Applicants' invention to combine the teachings from Bassett et al. and Yada et

al. to apply suitable ECC code to each block/area of a semiconductor-based memory

system, with an indicator indicative of whether a block is a reclaimed block and how

many times the block has been reused, in order to improve the performance and

reliability of the memory and to take advantage of the size benefit of a semiconductor-

based memory.

As to claim 6, it recites substantially the same limitations as in claim 4, and is

rejected based on the same reasons set forth in claim 4. Refer to "As to claim 4"

presented earlier in this Office Action. Further, Yada et al. that **the indicator has a**

value indicative of a number of times the block has been erased [Frequently-

rewritten parameter data is stored in the specified partial storage area, and program

data or the like low in rewriting frequency are stored in other storage areas (paragraph

0029); an electrically erasable and programmable non-volatile memory such as a flash

memory ... (paragraph 0002); thus, as writing/erasing for the flash memory is

repeatedly don... (paragraph 0005); the flash memory needs to be erased first before it

can be rewritten/reprogrammed again. Thus there is a one-to-one correspondence

between "the number of erasing" and "the number of rewriting/reprogramming," and the

frequency of rewriting is indicative of the frequency of erasing].

As to claim 7, Yada et al. that **the indicator has a value indicative of an**

approximately average number of times the blocks within the non-volatile

memory has been erased [Frequently-rewritten parameter data is stored in the

specified partial storage area, and program data or the like low in rewriting frequency

are stored in other storage areas (paragraph 0029)].

As to claim 9, Yada et al. teach that **the non-volatile memory is a flash**

memory [figure 3(A)~3(D) show the configuration of the flash memory array formed on

a semiconductor substrate; The data processing system can be implemented as a

single chip type microcomputer wherein the non-volatile memory and the central

processing unit are formed on a single semiconductor chip (paragraph 0031)].

As to claim 11, it recites substantially the same limitations as in claim 6, and is

rejected based on the same reasons set forth in claim 6. Refer to "As to claim 6"

presented earlier in this Office Action. Further, it is understood in the art that the same

error detection algorithm must be used for encoding and decoding to be able to recover

the original data correctly.

As to claim 16, it recites substantially the same limitations as in claim 6, and is

rejected based on the same reasons set forth in claim 6. Refer to "As to claim 6"

presented earlier in this Office Action.

As to claim 17, it recites substantially the same limitations as in claim 7, and is rejected based on the same reasons set forth in claim 7. Refer to "As to claim 7" presented earlier in this Office Action.

As to claim 19, it recites substantially the same limitations as in claim 9, and is rejected based on the same reasons set forth in claim 9. Refer to "As to claim 9" presented earlier in this Office Action.

As to claim 21, it recites substantially the same limitations as in claim 1, and is rejected based on the same reasons set forth in claim 1. Refer to "As to claim 1" presented earlier in this Office Action.

As to claim 26, it recites substantially the same limitations as in claim 6, and is rejected based on the same reasons set forth in claim 6. Refer to "As to claim 6" presented earlier in this Office Action.

As to claim 28, it recites substantially the same limitations as in claim 11, and is rejected based on the same reasons set forth in claim 11. Refer to "As to claim 11" presented earlier in this Office Action.

As to claim 31, it recites substantially the same limitations as in claim 4, and is rejected based on the same reasons set forth in claim 4. Refer to "As to claim 4" presented earlier in this Office Action.

As to claim 32, it recites substantially the same limitations as in claim 6, and is rejected based on the same reasons set forth in claim 6: Refer to "As to claim 6" presented earlier in this Office Action.

As to claim 33, it recites substantially the same limitations as in claim 6, and is rejected based on the same reasons set forth in claim 6. Refer to "As to claim 6" presented earlier in this Office Action.

As to claim 38, it recites substantially the same limitations as in claim 6, and is rejected based on the same reasons set forth in claim 6. Refer to "As to claim 6" presented earlier in this Office Action.

Claims 3, 13, 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), in view of Yada et al., US Patent Application Publication 2002/0032891), and further in view of Applicants' admission of prior art.

As to claims 3, 13, 23 and 30, Bassett et al. in view of Yada et al. does not explicitly mention that **the first algorithm is a 1-bit error correction code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm**.

However, 1-bit and 2-bit ECC are well known in the art, as evident by any textbook on the subject of error correction coding.

Further, figure 4 of Yada et al. shows a table of ECC with various number of ECC bits that may be used, depending the desired correcting capability,

Moreover, Applicants admit in the "Background of the Invention" section of their disclosure that both the 1-bit and 2-bit ECC algorithms are well known in the art (paragraph 0009).

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that both the 1-bit and 2-bit ECC algorithms

are well known in the art, as admitted by Applicants, hence lacking patentable

significance.

Claims 10, 20, 27 and 34 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Bassett et al. (US 6,747,827), in view of Yada et al., US Patent

Application Publication 2002/0032891), and further in view of Kramer (US 6,182,239).

As to claims 10, 20, 27 and 34, Bassett et al. in view of Yada et al. does not

explicitly mention that **the non-volatile memory is a flash memory, and particularly,**

one of a NAND flash memory and an MLC NAND flash memory.

However, the inventions of both Bassett et al. and Yada et al. are directly

applicable to any type of flash memories, including NAND flash memory and MLC

NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level

Memories" a fault-tolerant code semiconductor flash memory storage devices including

an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines

1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the

time of Applicants' invention to recognize that the particular limitation recited in this

claim is well known in the art, as demonstrated Kramer, hence lacking patentable

significance.

Claims 7, 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Bassett et al. (US 6,747,827), in view of Yada et al., US Patent Application

Publication 2002/0032891), and further in view of Bruce et al. (US 5,956,743).

As to claims 7, 8 and 18, Yada et al. teach that the selection of an ECC method matched with a device characteristic of each memory cell is enabled or allowed to obtain <u>a predetermined number of rewrite assurances</u>, and [paragraph 0012] and that <u>Frequently-rewritten</u> parameter data is stored in the specified partial storage area, and program data or the like <u>low in rewriting frequency</u> are stored in other storage areas [paragraph 0029]. But Bassett in view of Yada does not explicitly teach the data structure uses to store the indicator.

Further, Bruce et al. teach in their invention "Transparent Management at Host Interface of Flash-memory Overhead-Bytes Using Flash-Specific DMA Having Programmable Processor-Interrupt of High-Level Operations" a block management and replacement scheme for wear-leveling using ECC as part of the overhead bytes in a flash-memory chips [abstract] in which dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) [column 1, lines 57-67].

Using erase/write counters as indicators to support wear-leveling operations increases the life expectancy of a non-volatile memory device such as flash memory chip.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that benefit of using erase/write counters as indicators to support wear-leveling operation, as demonstrated Bruce et al., and to incorporate it into the existing scheme disclosed by Bassett et al. and Yada et al. to further improve the life expectancy of the non-volatile memory devices.

As to claim 7, Bruce et al. teach that **the indicator is arranged to indicate an approximately average number of times blocks within the non-volatile memory have been erased** [dual write counters are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 8, Bruce et al. teach that **the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator from the data structure** [the data structure is the dual write counters that are allocated to each of the block to indicate how many times a block has been erased and written (i.e., reclaimed) (column 1, lines 57-67)].

As to claim 17, it recites substantially the same limitations as in claim 7, and is rejected based on the same reasons set forth in claim 7. Refer to "As to claim 7" presented earlier in this Office Action.

As to claim 18, it recites substantially the same limitations as in claim 6, and is rejected based on the same reasons set forth in claim 6. Refer to "As to claim 4" presented earlier in this Office Action.

(10) Response to Arguments

Appellants' arguments have been fully and carefully considered with Examiner's answers set forth below.

Response to Argument on Claim 4 and its dependent claim 3

Appellants contend that Bassett in view of Yada fails to teach the existence of an indicator, associated with a block of non-volatile memory, that is indicative of whether that block is a reclaimed block, much less than select an error detection algorithm responsive to this indicator. The Examiner disagrees.

First, the inventions of both Bassett and Yada are directed to selecting an error detection algorithm for each of a plurality of regions based on attributes associated with each region.

Bessett teaches that [For example, different error correcting codes of different strengths may be applied on a sector-by-sector basis, or on some other basis, depending upon the particular application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the physical location of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms preferably produce a different number of error correction code bits for application to the data (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by Yada [The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method matched with a device characteristic of each memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, as for the indication of whether a block/sector/region is "a reclaimed block," it is noted that the citing of "a reclaimed block" only appears as part of preamble stating the purpose and intended use of claim 4, and the context of the body of the claim does not even refer to "a reclaimed block" at all. As such, the element "a reclaimed block" does not carry weight and is not to be considered when determining its patentability with respect to prior art. See MPEP 2111.02 [R-3], "Effect of Preamble," Section II.

Even if the element "a reclaimed block" is to be considered as a claim limitation, it is taught by reference Yada anyway. Here the Examiner interprets "a reclaimed block" as "a reused block," and Yada teaches that the selection of a particular ECC method depends on the frequency of reuse of a memory block [the addition of ECC codes and

an error correction are performed to increase <u>the number of rewrite assurances</u> with

only an access to data stored in <u>a specified partial storage area</u> of a non-volatile

memory as an object. <u>Frequently-rewritten</u> parameter data is stored in <u>the specified</u>

<u>partial storage area</u>, and program data or the like <u>low in rewriting frequency</u> are stored

in <u>other storage areas</u> (paragraph 0029)].

Thus, Yada clearly teaches that "the specified partial storage area" is an area

that is subjected to high frequency of "reuse" via "rewriting" of certain data while "other

storage areas" is subjected to low frequency of "reuse," and the application of ECC

codes depends on which area is under consideration. The frequency of reuse is

certainly an indication of how often a block/area is being reused.

Appellants also contend that the "frequently-rewritten" modifier only applies to the

"nature of the data" and does not applied to "the destination block." The Examiner

disagrees.

First, Yada teaches that "the specified partial storage area" is used to store

"Frequently-rewritten parameter data" and "other storage areas" are used to store

"program data or the like low in rewriting frequency." In other words, the characteristics

of an area is taken into consideration to match up with the nature of data [The present

inventors have paid attention to <u>the difference between the individual memory cell</u>

<u>characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that <u>the selection of an ECC method matched with a device characteristic of each</u>

memory cell is enabled or allowed to obtain a predetermined number of rewrite
assurances, and overhead of each ECC code for the data is reduced, whereby the use
efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy,
"glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash"
goes into "a garbage can." Thus, there is a direct correspondence between "the nature
of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in
another way, "the nature of the objects/data" is also a direct reflection, or an indication,
of the nature of the corresponding "storage areas." After all, it is only normal to deposit
"valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the
other way around.

Appellants also contend that there is no suggestion to combine the teachings
from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to
selecting a suitable error detection algorithm (ECC) for each of a plurality of
regions/areas based on attributes associated with each region/area. Thus, they share
the same common goal of efficiently applying ECC code to a region/area of memory
storage space in order to minimize the overhead associated with the ECC code.
Therefore, persons of ordinary skills in the art interested in solving the common problem
of "selecting a suitable error detection algorithm (ECC) for each of a plurality of
regions/areas based on attributes associated with each region/area" would have

combined the teachings from Bassett and Yada to tailor their unique needs, be it on a semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim 4. As such, the Examiner's position regarding the patentability of claim 4 and its dependent claim 3 remains the same as stated in the previous Office Action.

Response to Argument on Claim 6 and its dependent claims 7-11 and 13

Independent claim 6 recites substantially the same limitations as independent claim 4, with the difference in that "the indicator" in claim 6 "has a value indicative of a number of times the first block has been erased," instead of being "indicative of whether the block is a reclaimed block" as recited in claim 4.

Appellants again contend that Bassett in view of Yada fails to teach the encoding of data according to a first or a second error detection algorithm, of different error capacity, according to any attribute of the destination block in an array formed on a semiconductor substrate, much less responsive to an indicator having a value indicative of a number of times the first block has been erased. The Examiner disagrees.

The Examiner will address the aspect of "the encoding of data according to a first or a second error detection algorithm, of different error capacity, according to any attribute of the destination block in an array formed on a semiconductor substrate" to being with.

First, the inventions of both Bassett and Yada are directed to selecting an error detection algorithm for each of a plurality of regions based on attributes associated with each region.

Bessett teaches that [For example, <u>different error correcting codes</u> of different

strengths may be applied <u>on a sector-by-sector basis</u>, or on some other basis,

depending upon the particular application, data types involved, and so forth (column 7,

lines 29-33); the error correction selection criterion selects <u>which of said first and</u>

<u>second algorithms</u> is to be applied in dependence upon <u>the physical location</u> of said

data on said hard disk drive. In another embodiment, the error correction selection

criterion selects which of said first and second algorithms is to be applied in

dependence upon the type of said data to be written to the disk. <u>The first and second</u>

<u>error correction code algorithms preferably produce a different number of error</u>

<u>correction code bits for application to the data</u> (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage

disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection

mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by

Yada [The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are

formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to <u>the difference</u>

<u>between the individual memory cell characteristics</u> and thereby have fount out utility in

that the number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory. In short, the present

inventors have found out utility in that <u>the selection of an ECC method matched with a</u>

<u>device characteristic of each memory cell</u> is enabled or allowed to obtain a

predetermined number of rewrite assurances, and overhead of each ECC code for the

data is reduced, whereby the use efficiency of the storage area is set to the maximum

(paragraph 0012)].

Second, as for the aspect of "according to any attribute of the destination block in

an array formed on a semiconductor substrate," Yada teaches that [The present

inventors have paid attention to the difference between the individual memory cell

characteristics and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that the selection of an ECC method matched with a device characteristic of each

memory cell is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use

efficiency of the storage area is set to the maximum (paragraph 0012)].

Thus, Yada clearly teaches "paying attention to the difference between the

individual memory cell characteristics and thereby have fount out utility in that the

number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory." Note that

"characteristics" of individual memory cell is the corresponding "attributes" of a memory

cell.

Third, as for the aspect of "an indicator having a value indicative of a number of

times the first block has been erased," Yada teaches the selection of a particular ECC

method depends on the frequency of reuse of a memory block [the addition of ECC

codes and an error correction are performed to increase <u>the number of rewrite</u> <u>assurances</u> with only an access to data stored in <u>a specified partial storage area</u> of a non-volatile memory as an object. <u>Frequently-rewritten</u> parameter data is stored in <u>the</u> <u>specified partial storage area</u>, and program data or the like <u>low in rewriting frequency</u> are stored in <u>other storage areas</u> (paragraph 0029); the present invention has a <u>first</u> <u>storage area</u> (20Bb) <u>low in</u> <u>the number of rewrite assurances</u>, and a <u>second storage</u> <u>area</u> (20Ba) <u>high in</u> <u>the number of rewrite assurances</u> (paragraph 0042)].

Further, Yada's invention is directed toward a flash memory, and a flash memory needs to be erased first before it can be rewritten again [an electrically <u>erasable</u> and <u>programmable</u> non-volatile memory such as a flash memory ... (paragraph 0002); thus, as writing/erasing for the flash memory is repeatedly done... (paragraph 0005)]. Thus there is a one-to-one correspondence between "the number of erasing" and "the number of rewriting," and the frequency of rewriting is indicative of the frequency of erasing.

It is noted that, by definition, "the frequency" of any event (e.g., reuse/erase/rewrite) is derived directly from "the number of occurrence" of that event (e.g., reuse/erase/rewrite) over a period of time. Therefore, the frequency of reuse of a block serves as an indication of the number of times the block is erased as far as a flash memory is concerned.

Appellants again contend that the "frequently-rewritten" modifier only applies to the "nature of the data" and does not applied to "the destination block." The Examiner disagrees.

First, Yada teaches that "the specified partial storage area" is used to store "Frequently-rewritten parameter data" and "other storage areas" are used to store "program data or the like low in rewriting frequency." In other words, the characteristics of an area is taken into consideration to match up with the nature of data [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method</u> matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy, "glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash" goes into "a garbage can." Thus, there is a direct correspondence between "the nature of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in another way, "the nature of the objects/data" is also a direct reflection, or an indication, of the nature of the corresponding "storage areas." After all, it is only normal to deposit "valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the other way around.

Appellants also contend that there is no suggestion to combine the teachings from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area. Thus, they share the same common goal of efficiently applying ECC code to a region/area of memory storage space in order to minimize the overhead associated with the ECC code. Therefore, persons of ordinary skills in the art interested in solving the common problem of "selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area" would have combined the teachings from Bassett and Yada to tailor their unique needs, be it on a semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim 6. As such, the Examiner's position regarding the patentability of claim 6 and all its dependent claims remains the same as stated in the previous Office Action.

Response to Argument on Claim 16 and its dependent claims 17-20

Independent claim 16 recites substantially the same limitations as independent claim 6, with both of them citing, besides other limitations, "an indicator having a value indicative of a number of times the first block has been erased."

Appellants once again contend that Bassett in view of Yada fails to teach the encoding of data according to a first or a second error detection algorithm, of different error capacity, according to any attribute of the destination block in an array formed on a semiconductor substrate, much less responsive to an indicator having a value indicative of a number of times the first block has been erased. The Examiner disagrees.

The Examiner will address the aspect of "the encoding of data according to a first or a second error detection algorithm, of different error capacity, according to any attribute of the destination block in an array formed on a semiconductor substrate" to being with.

First, the inventions of both Bassett and Yada are directed to selecting an error detection algorithm for each of a plurality of regions based on attributes associated with each region.

Bessett teaches that [For example, different error correcting codes of different strengths may be applied on a sector-by-sector basis, or on some other basis, depending upon the particular application, data types involved, and so forth (column 7, lines 29-33); the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the physical location of said data on said hard disk drive. In another embodiment, the error correction selection criterion selects which of said first and second algorithms is to be applied in dependence upon the type of said data to be written to the disk. The first and second error correction code algorithms preferably produce a different number of error correction code bits for application to the data (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by Yada [The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method matched with a device characteristic of each memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, as for the aspect of "according to any attribute of the destination block in an array formed on a semiconductor substrate," Yada teaches that [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method matched with a device characteristic of each memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Thus, Yada clearly teaches "paying attention to <u>the difference between the</u>

<u>individual memory cell characteristics</u> and thereby have fount out utility in that the

number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory." Note that

"characteristics" of individual memory cell is the corresponding "attributes" of a memory

cell.

Third, as for the aspect of "an indicator having a value indicative of a number of

times the first block has been erased," Yada teaches the selection of a particular ECC

method depends on the frequency of reuse of a memory block [the addition of ECC

codes and an error correction are performed to increase <u>the number of rewrite</u>

<u>assurances</u> with only an access to data stored in <u>a specified partial storage area</u> of a

non-volatile memory as an object. <u>Frequently-rewritten</u> parameter data is stored in <u>the</u>

<u>specified partial storage area</u>, and program data or the like <u>low in rewriting frequency</u>

are stored in <u>other storage areas</u> (paragraph 0029); the present invention has a <u>first</u>

<u>storage area</u> (20Bb) <u>low in</u> the number of rewrite assurances, and a <u>second storage</u>

<u>area</u> (20Ba) <u>high in</u> the number of rewrite assurances (paragraph 0042)].

Further, Yada's invention is directed toward a flash memory, and a flash memory

needs to be erased first before it can be rewritten again [an electrically <u>erasable</u> and

<u>programmable</u> non-volatile memory such as a flash memory ... (paragraph 0002); thus,

as writing/erasing for the flash memory is repeatedly done... (paragraph 0005)]. Thus

there is a one-to-one correspondence between "the number of erasing" and "the

number of rewriting," and the frequency of rewriting is indicative of the frequency of erasing.

It is noted that, by definition, "the frequency" of any event (e.g., reuse/erase/rewrite) is derived directly from "the number of occurrence" of that event (e.g., reuse/erase/rewrite) over a period of time. Therefore, the frequency of reuse of a block serves as an indication of the number of times the block is erased as far as a flash memory is concerned.

Appellants again contend that the "frequently-rewritten" modifier only applies to the "nature of the data" and does not applied to "the destination block." The Examiner disagrees.

First, Yada teaches that "the specified partial storage area" is used to store "Frequently-rewritten parameter data" and "other storage areas" are used to store "program data or the like low in rewriting frequency." In other words, the characteristics of an area is taken into consideration to match up with the nature of data [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method</u> matched with a device characteristic of each memory cell is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy, "glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash" goes into "a garbage can." Thus, there is a direct correspondence between "the nature of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in another way, "the nature of the objects/data" is also a direct reflection, or an indication, of the nature of the corresponding "storage areas." After all, it is only normal to deposit "valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the other way around.

Appellants also contend that there is no suggestion to combine the teachings from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area. Thus, they share the same common goal of efficiently applying ECC code to a region/area of memory storage space in order to minimize the overhead associated with the ECC code. Therefore, persons of ordinary skills in the art interested in solving the common problem of "selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area" would have combined the teachings from Bassett and Yada to tailor their unique needs, be it on a semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim

16. As such, the Examiner's position regarding the patentability of claim 16 and all its

dependent claims remains the same as stated in the previous Office Action.

Response to Argument on Claim 21 and its dependent claims 23 and 27-32

Independent claim 21 recites substantially the same limitations as independent

claim 4, with both of them citing, besides other limitations, "an indicator having a value

indicative of whether a block is a reclaimed block."

Appellants contend that Bassett in view of Yada fails to teach the existence of an

indicator, associated with a block of non-volatile memory, that is indicative of whether

that block is a reclaimed block, much less than select an error detection algorithm

responsive to this indicator. The Examiner disagrees.

First, the inventions of both Bassett and Yada are directed to selecting an error

detection algorithm for each of a plurality of regions based on attributes associated with

each region.

Bessett teaches that [For example, different error correcting codes of different

strengths may be applied on a sector-by-sector basis, or on some other basis,

depending upon the particular application, data types involved, and so forth (column 7,

lines 29-33); the error correction selection criterion selects which of said first and

second algorithms is to be applied in dependence upon the physical location of said

data on said hard disk drive. In another embodiment, the error correction selection

criterion selects which of said first and second algorithms is to be applied in

dependence upon the type of said data to be written to the disk. The first and second

error correction code algorithms preferably produce a different number of error

correction code bits for application to the data (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage

disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection

mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by

Yada [The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are

formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to the difference

between the individual memory cell characteristics and thereby have fount out utility in

that the number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory. In short, the present

inventors have found out utility in that the selection of an ECC method matched with a

device characteristic of each memory cell is enabled or allowed to obtain a

predetermined number of rewrite assurances, and overhead of each ECC code for the

data is reduced, whereby the use efficiency of the storage area is set to the maximum

(paragraph 0012)].

Second, as for the indication of whether a block/sector/region is a reclaimed

block, the Examiner interprets "a reclaimed block" as "a reused block," and Yada

teaches that the selection of a particular ECC method depends on the frequency of

reuse of a memory block [the addition of ECC codes and an error correction are

performed to increase the number of rewrite assurances with only an access to data

stored in <u>a specified partial storage area</u> of a non-volatile memory as an object.

<u>Frequently-rewritten</u> parameter data is stored in <u>the specified partial storage area</u>, and

program data or the like <u>low in rewriting frequency</u> are stored in <u>other storage areas</u>

(paragraph 0029)].

Thus, Yada clearly teaches that "the specified partial storage area" is an area

that is subjected to high frequency of "reuse" via "rewriting" of certain data while "other

storage areas" is subjected to low frequency of "reuse," and the application of ECC

codes depends on which area is under consideration. The frequency of reuse is

certainly an indication of how often a block/area is being reused.

Appellants also contend that the "frequently-rewritten" modifier only applies to the

"nature of the data" and does not applied to "the destination block." The Examiner

disagrees.

First, Yada teaches that "the specified partial storage area" is used to store

"Frequently-rewritten parameter data" and "other storage areas" are used to store

"program data or the like low in rewriting frequency." In other words, the characteristics

of an area is taken into consideration to match up with the nature of data [The present

inventors have paid attention to <u>the difference between the individual memory cell</u>

<u>characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that <u>the selection of an ECC method</u> <u>matched with a device characteristic of each</u>

<u>memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy, "glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash" goes into "a garbage can." Thus, there is a direct correspondence between "the nature of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in another way, "the nature of the objects/data" is also a direct reflection, or an indication, of the nature of the corresponding "storage areas." After all, it is only normal to deposit "valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the other way around.

Appellants also contend that there is no suggestion to combine the teachings from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area. Thus, they share the same common goal of efficiently applying ECC code to a region/area of memory storage space in order to minimize the overhead associated with the ECC code. Therefore, persons of ordinary skills in the art interested in solving the common problem of "selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area" would have combined the teachings from Bassett and Yada to tailor their unique needs, be it on a semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim

21. As such, the Examiner's position regarding the patentability of claim 21 and its

dependent claim 3 remains the same as stated in the previous Office Action.

Response to Argument on Claim 26

Independent claim 26 recites substantially the same limitations as independent

claims 6 and 16, with all of them citing, besides other limitations, "an indicator having a

value indicative of a number of times the first block has been erased."

Appellants once more contend that Bassett in view of Yada fails to teach the

encoding of data according to a first or a second error detection algorithm, of different

error capacity, according to any attribute of the destination block in an array formed on a

semiconductor substrate, much less responsive to an indicator having a value indicative

of a number of times the first block has been erased. The Examiner disagrees.

The Examiner will address the aspect of "the encoding of data according to a first

or a second error detection algorithm, of different error capacity, according to any

attribute of the destination block in an array formed on a semiconductor substrate" to

being with.

First, the inventions of both Bassett and Yada are directed to selecting an error

detection algorithm for each of a plurality of regions based on attributes associated with

each region.

Bessett teaches that [For example, different error correcting codes of different

strengths may be applied on a sector-by-sector basis, or on some other basis,

depending upon the particular application, data types involved, and so forth (column 7,

lines 29-33); the error correction selection criterion selects <u>which of said</u> <u>first and</u>

<u>second algorithms</u> is to be applied in dependence upon <u>the physical location</u> of said

data on said hard disk drive. In another embodiment, the error correction selection

criterion selects which of said first and second algorithms is to be applied in

dependence upon the type of said data to be written to the disk. <u>The first and second</u>

<u>error correction code algorithms preferably produce a different number of error</u>

<u>correction code bits for application to the data</u> (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage

disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection

mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by

Yada [The data processing system can be implemented as a single chip type

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formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to <u>the difference</u>

<u>between the individual memory cell characteristics</u> and thereby have fount out utility in

that the number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory. In short, the present

inventors have found out utility in that <u>the selection of an ECC method</u> <u>matched with a</u>

<u>device characteristic of each memory cell</u> is enabled or allowed to obtain a

predetermined number of rewrite assurances, and overhead of each ECC code for the

data is reduced, whereby the use efficiency of the storage area is set to the maximum

(paragraph 0012)].

Second, as for the aspect of "according to any attribute of the destination block in an array formed on a semiconductor substrate," Yada teaches that [The present inventors have paid attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory. In short, the present inventors have found out utility in that <u>the selection of an ECC method</u> <u>matched with a device characteristic of each memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite assurances, and overhead of each ECC code for the data is reduced, whereby the use efficiency of the storage area is set to the maximum (paragraph 0012)].

Thus, Yada clearly teaches "paying attention to <u>the difference between the individual memory cell characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes corresponding to the number of data bits can be determined according to the characteristic of the flash memory." Note that "characteristics" of individual memory cell is the corresponding "attributes" of a memory cell.

Third, as for the aspect of "an indicator having a value indicative of a number of times the first block has been erased," Yada teaches the selection of a particular ECC method depends on the frequency of reuse of a memory block [the addition of ECC codes and an error correction are performed to increase <u>the number of rewrite assurances</u> with only an access to data stored in <u>a specified partial storage area</u> of a non-volatile memory as an object. <u>Frequently-rewritten</u> parameter data is stored in <u>the</u>

specified partial storage area, and program data or the like low in rewriting frequency

are stored in other storage areas (paragraph 0029); the present invention has a first

storage area (20Bb) low in the number of rewrite assurances, and a second storage

area (20Ba) high in the number of rewrite assurances (paragraph 0042)].

Further, Yada's invention is directed toward a flash memory, and a flash memory

needs to be erased first before it can be rewritten again [an electrically erasable and

programmable non-volatile memory such as a flash memory ... (paragraph 0002); thus,

as writing/erasing for the flash memory is repeatedly done... (paragraph 0005)]. Thus

there is a one-to-one correspondence between "the number of erasing" and "the

number of rewriting," and the frequency of rewriting is indicative of the frequency of

erasing.

It is noted that, by definition, "the frequency" of any event (e.g.,

reuse/erase/rewrite) is derived directly from "the number of occurrence" of that event

(e.g., reuse/erase/rewrite) over a period of time. Therefore, the frequency of reuse of a

block serves as an indication of the number of times the block is erased as far as a flash

memory is concerned.

Appellants again contend that the "frequently-rewritten" modifier only applies to

the "nature of the data" and does not applied to "the destination block." The Examiner

disagrees.

First, Yada teaches that "the specified partial storage area" is used to store

"Frequently-rewritten parameter data" and "other storage areas" are used to store

"program data or the like low in rewriting frequency." In other words, the characteristics

of an area is taken into consideration to match up with the nature of data [The present

inventors have paid attention to the difference between the individual memory cell

characteristics and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that the selection of an ECC method matched with a device characteristic of each

memory cell is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use

efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy,

"glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash"

goes into "a garbage can." Thus, there is a direct correspondence between "the nature

of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in

another way, "the nature of the objects/data" is also a direct reflection, or an indication,

of the nature of the corresponding "storage areas." After all, it is only normal to deposit

"valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the

other way around.

Appellants also contend that there is no suggestion to combine the teachings

from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to

selecting a suitable error detection algorithm (ECC) for each of a plurality of

regions/areas based on attributes associated with each region/area. Thus, they share

the same common goal of efficiently applying ECC code to a region/area of memory

storage space in order to minimize the overhead associated with the ECC code.

Therefore, persons of ordinary skills in the art interested in solving the common problem

of "selecting a suitable error detection algorithm (ECC) for each of a plurality of

regions/areas based on attributes associated with each region/area" would have

combined the teachings from Bassett and Yada to tailor their unique needs, be it on a

semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim

26. As such, the Examiner's position regarding the patentability of claim 26 and all its

dependent claims remains the same as stated in the previous Office Action.

Response to Argument on Claim 33 and its dependent claim 34

Independent claim 33 recites substantially the same limitations as independent

claims 6, 16 and 26, with all of them citing, besides other limitations, "an indicator

having a value indicative of a number of times the first block has been erased."

Appellants again contend that Bassett in view of Yada fails to teach the encoding

of data according to a first or a second error detection algorithm, of different error

capacity, according to any attribute of the destination block in an array formed on a

semiconductor substrate, much less responsive to an indicator having a value indicative

of a number of times the first block has been erased. The Examiner disagrees.

The Examiner will address the aspect of "the encoding of data according to a first

or a second error detection algorithm, of different error capacity, according to any

attribute of the destination block in an array formed on a semiconductor substrate" to

being with.

First, the inventions of both Bassett and Yada are directed to selecting an error

detection algorithm for each of a plurality of regions based on attributes associated with

each region.

Bessett teaches that [For example, different error correcting codes of different

strengths may be applied on a sector-by-sector basis, or on some other basis,

depending upon the particular application, data types involved, and so forth (column 7,

lines 29-33); the error correction selection criterion selects which of said first and

second algorithms is to be applied in dependence upon the physical location of said

data on said hard disk drive. In another embodiment, the error correction selection

criterion selects which of said first and second algorithms is to be applied in

dependence upon the type of said data to be written to the disk. The first and second

error correction code algorithms preferably produce a different number of error

correction code bits for application to the data (column 2, lines 37-46)].

The Examiner acknowledges that Bessett's invention is directed to a storage

disk, which may not be a semiconductor substrate [refer to page 7 of the Final Rejection

mailed on 9/19/2006]. However, the aspect of semiconductor substrate is taught by

Yada [The data processing system can be implemented as a single chip type

microcomputer wherein the non-volatile memory and the central processing unit are

formed on a single semiconductor chip (paragraph 0031)].

Yada teaches that [The present inventors have paid attention to <u>the difference</u>

<u>between the individual memory cell characteristics</u> and thereby have fount out utility in

that the number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory. In short, the present

inventors have found out utility in that <u>the selection of an ECC method</u> <u>matched with a</u>

<u>device characteristic of each memory cell</u> is enabled or allowed to obtain a

predetermined number of rewrite assurances, and overhead of each ECC code for the

data is reduced, whereby the use efficiency of the storage area is set to the maximum

(paragraph 0012)].

Second, as for the aspect of "according to any attribute of the destination block in

an array formed on a semiconductor substrate," Yada teaches that [The present

inventors have paid attention to <u>the difference between the individual memory cell</u>

<u>characteristics</u> and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that <u>the selection of an ECC method</u> <u>matched with a device characteristic of each</u>

<u>memory cell</u> is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use

efficiency of the storage area is set to the maximum (paragraph 0012)].

Thus, Yada clearly teaches "paying attention to <u>the difference between the</u>

<u>individual memory cell characteristics</u> and thereby have fount out utility in that the

number of bits of ECC codes corresponding to the number of data bits can be

determined according to the characteristic of the flash memory." Note that

"characteristics" of individual memory cell is the corresponding "attributes" of a memory

cell.

Third, as for the aspect of "an indicator having a value indicative of a number of

times the first block has been erased," Yada teaches the selection of a particular ECC

method depends on the frequency of reuse of a memory block [the addition of ECC

codes and an error correction are performed to increase <u>the number of rewrite</u>

<u>assurances</u> with only an access to data stored in <u>a specified partial storage area</u> of a

non-volatile memory as an object. <u>Frequently-rewritten</u> parameter data is stored in <u>the</u>

<u>specified partial storage area</u>, and program data or the like <u>low in rewriting frequency</u>

are stored in <u>other storage areas</u> (paragraph 0029); the present invention has a <u>first</u>

<u>storage area</u> (20Bb) <u>low in</u> the number of rewrite assurances, and a <u>second storage</u>

<u>area</u> (20Ba) <u>high in</u> the number of rewrite assurances (paragraph 0042)].

Further, Yada's invention is directed toward a flash memory, and a flash memory

needs to be erased first before it can be rewritten again [an electrically <u>erasable</u> and

<u>programmabl</u>e non-volatile memory such as a flash memory ... (paragraph 0002); thus,

as writing/erasing for the flash memory is repeatedly done... (paragraph 0005)]. Thus

there is a one-to-one correspondence between "the number of erasing" and "the

number of rewriting," and the frequency of rewriting is indicative of the frequency of

erasing.

It is noted that, by definition, "the frequency" of any event (e.g.,

reuse/erase/rewrite) is derived directly from "the number of occurrence" of that event

(e.g., reuse/erase/rewrite) over a period of time. Therefore, the frequency of reuse of a

block serves as an indication of the number of times the block is erased as far as a flash

memory is concerned.

Appellants again contend that the "frequently-rewritten" modifier only applies to

the "nature of the data" and does not applied to "the destination block." The Examiner

disagrees.

First, Yada teaches that "the specified partial storage area" is used to store

"Frequently-rewritten parameter data" and "other storage areas" are used to store

"program data or the like low in rewriting frequency." In other words, the characteristics

of an area is taken into consideration to match up with the nature of data [The present

inventors have paid attention to the difference between the individual memory cell

characteristics and thereby have fount out utility in that the number of bits of ECC codes

corresponding to the number of data bits can be determined according to the

characteristic of the flash memory. In short, the present inventors have found out utility

in that the selection of an ECC method matched with a device characteristic of each

memory cell is enabled or allowed to obtain a predetermined number of rewrite

assurances, and overhead of each ECC code for the data is reduced, whereby the use

efficiency of the storage area is set to the maximum (paragraph 0012)].

Second, using the common practice of "recycling" material as an analogy,

"glass/plastic/aluminum objects" are placed into "a designated recycle bin" while "trash"

goes into "a garbage can." Thus, there is a direct correspondence between "the nature

of the objects/data" and "the nature of the bin/can/storage areas," or, to state it in

another way, "the nature of the objects/data" is also a direct reflection, or an indication, of the nature of the corresponding "storage areas." After all, it is only normal to deposit "valuable jewelry" in "a safety box" and to place "trash" in "a garbage can," and not the other way around.

Appellants also contend that there is no suggestion to combine the teachings from Bessett and Yada. The Examiner disagrees.

As presented earlier, the inventions of both Bassett and Yada are directed to selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area. Thus, they share the same common goal of efficiently applying ECC code to a region/area of memory storage space in order to minimize the overhead associated with the ECC code. Therefore, persons of ordinary skills in the art interested in solving the common problem of "selecting a suitable error detection algorithm (ECC) for each of a plurality of regions/areas based on attributes associated with each region/area" would have combined the teachings from Bassett and Yada to tailor their unique needs, be it on a semiconductor substrate or on a disk.

Therefore, Bessett in view of Yada indeed teach all the limitations recited in claim 33. As such, the Examiner's position regarding the patentability of claim 33 and all its dependent claims remains the same as stated in the previous Office Action.

(11) Related Proceedings Appendix

None.

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